United States Patent [19]

Ohuchi

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[54] **MEMORY DEVICE**

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[58] **Field of Search** ... 364/200 MS File, 900 MS File

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[57] **ABSTRACT**

A memory device coupled to a data flow processor inserted in token ring. Its operation is initiated upon receiving incoming tokens including an instruction code and information. The instruction code includes a memory read instruction, a memory write instruction, an extended address set instruction, and a write data set instruction. The memory device comprises a memory unit, a first register for holding a data, a second register for holding an extended address, and control circuitry operative to control each operation of the memory unit and the registers. Thus, when the control circuitry decodes the memory write and memory read instructions, the data stored in the first register is written into the memory unit in response to an address set of a combination of the extended address and subsequently received address, and a data stored in the memory unit is read out of the memory unit in response to the address set, respectively, when the control circuitry decodes the extended address set instruction, information is set in the second register as an address, and when the control circuitry decodes the write data set instruction, information is set in the first register as a data.

12 Claims, 2 Drawing Sheets